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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,594	12/27/2000	Terry L. Kendall	42390P10071	1642

7590 07/02/2003

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EXAMINER
GOSSAGE, GLENN A

ART UNIT	PAPER NUMBER
2187	11

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,594	KENDALL ET AL.	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 December 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 and 10 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A new title such as --METHOD AND APPARATUS INCLUDING SPECIAL PROGRAMMING MODE CIRCUITRY WHICH DISABLES INTERNAL PROGRAM VERIFY OPERATIONS BY A MEMORY-- is suggested (see claim 1, lines 1 and 5 and claim 13, lines 1 and 4-5, e.g.). The loss in brevity of title is more than offset by the gain in its informative value in indexing, classifying, searching, etc. See MPEP 606 and 606.01.

2. The abstract of the disclosure is objected to because in lines 1-2, it appears " . The special programming mode disables internal" should be changed to --and internal program--, and --is disabled-- inserted after "memory" in line 2, for clarity and consistency (see lines 4-5 and 5-6, e.g.). Also, it appears the last sentence ("An apparatus ... mode circuitry.") should be moved before "The" in line 2 so that one can quickly determine from a cursory inspection the nature and gist of the technical disclosure as required by 37 CFR 1.72(b).

One or two sentences should be added describing additionally claimed and disclosed features. [For example, in line 6, after "enabled.", insert a sentence such as --The special programming mode may use hashing to optimize testing for a memory such as a nonvolatile flash memory.-- (see page 2, lines 5-8 and page 9, lines 2-6.]

Appropriate correction is required. See MPEP § 608.01(b).

3. The drawings are objected to because in Figure 2, at the top of the Figure, it appears "(4) START" should be simply --START-- for clarity.

In Figure 4, descriptive labels should be added within each of the "boxes" for clarity (as is done in Fig. 5, e.g.), particularly since this Figure shows a host processor coupled to a flash memory including special programming mode circuitry in accordance with an embodiment of the present invention. [By way of example, labels such as --HOST COMPUTER--, --FLASH MEMORY-- and --CONTROL CIRCUITRY-- should be added near the "top" inside of "boxes" 22, 24 and 28, respectively, for clarity (see page 10, lines 1-2 and 13, e.g.). Similarly, labels such as --FLASH MEMORY ARRAY--; -- SPEC. PROG. MODE CCTY. -- ; --PROC. CCTY.-- ; and --MEMORY (DRAM)-- should be added within "boxes" 20, 32, 33 and 34, respectively, for clarity (see page 10, lines 1 and 13-15, e.g.).]

In Figure 5, a descriptive label (such as --SPEC. PROG. MODE--) should be added within "box" 32 for clarity.

Similarly, in Figure 6, a descriptive label (such as --SPEC. PROG. MODE--) should be added within "box" 32 for clarity. Also, in "box" 40, it appears "CUI" should be written out (as --COMMAND USER INTERFACE--) for clarity, since the acronym "CUI" is not well known or commonly used in the art, and consistency (with Figure 5, e.g.). The acronym "WSM" may also be written out (as --WRITE STATE MACH.-- , e.g.) for clarity. In "boxes" 62 and 91, it appears "QUEUE" should be deleted for consistency (see page 12, line 2 and page 15, line 23, e.g.).

Within "box" 83, it appears "REGISTERS" should be --REGISTER-- for consistency (with page 16, line 8 and Figure 5, e.g.).

In Figure 7, within "block" 164, "NODE" should be --MODE-- (see page 34, line 19, e.g.).

In Figure 9B, within decision block 317, it appears --WORD-- should be inserted after "DATA" for clarity and consistency (see Figure 9A, e.g.).

Applicant is REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) (submission of corrected formal drawings, e.g.) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "circuit to send," which is within the host processor, and "circuit to exit," of claim 13; the "circuit to verify," within the host processor, of claim 14; and the "circuitry to determine" (within the "circuit to verify"?) of claim 17; the "circuit to reprogram" of claim 18; and the "circuit one word that did not verify" (?) of claim 19, must be shown or the features canceled from the claims. No new matter should be entered.

5. The disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any

errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 1, it appears a cross-reference to the related applications cited in the letter filed June 21, 2001 under 37 CFR 1.78, should be between lines 2 and 3 for clarity (in this regard, see MPEP 608.01(a) and (b)).

On page 3, line 21, it appears "program" should be --programming-- for clarity and consistency (see line 16, e.g.).

On page 10, line 5, it appears --(PDA)-- should be inserted after "assistant" for clarity.

On page 11, line 6, and throughout the specification, the first occurrence of all acronyms or abbreviations should be written out for clarity, whether or not they may be considered "well known." Accordingly, "DRAM" should be changed to --dynamic random access memory (DRAM)-- for clarity. In line 21, it appears "a" (second occurrence) should be deleted for clarity.

On page 12, line 21, it appears --flash memory-- should be inserted before "device" for consistency (note lines 14 and 16, e.g.).

On page 14, line 6, "requiring program or a" appears to read more clearly here as --requiring programming or to--.

On page 15, line 5, it appears --(102, 104, 106)-- should be inserted after "26" for clarity. In line 13, it appears "prevents the" should be --prevents internal-- for clarity and consistency (see page 18, lines 20-21, e.g.). In line 15, it appears "the" should be --a--.

On page 16, lines 17 and 19, it appears "117a-117p" should be --117A-117P-- for consistency (with Figure 6). See also page 29, lines 5, 7, 8 and 10.

On page 20, line 14, it appears --the-- should be inserted before "address (first occurrence) for clarity.

On page 29, line 7, it appears 'of" (second occurrence) should be deleted. In line 8, --a-- should be inserted after "then" for clarity.

On page 33, lines 20-21, "an exit" should be --an exit--. See also page 34, lines 15-16.

On page 34, line 16, it appears a reference to a specific Figure should be made for clarity.

On page 35, line 6, it appears "then" should be deleted for clarity.

On page 36, lines 9-10, it is not understood what is meant by "the last data is checked in process block 308" here.

On page 37, line 9, "an" should be --a--. In line 13, it appears --or procedures-- should be inserted before "320" for consistency (see line 9, e.g.). Similarly, it appears --for procedure-- should be inserted before "320" in line 17 for consistency (again see line 9, e.g.). See also page 39, lines 12 and 17; page 40, line 18; and page 41, lines 4 and 10.

On page 40, line 16, it appears "compare" reads more clearly here as --are the same--.

On page 41, line 21, it appears --circuitry-- should be inserted before "32" for clarity and consistency.

On page 43, line 2, it appears --or lines-- should be inserted before "26" for consistency (see page 10, line 2, e.g.). In line 5, "state and" should be --state, and-- for clarity.

On page 44, line 16, "a" should be --an--. In line 17, it appears --(Fig. 17)-- should be inserted after "160" for clarity..

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 2, line 3, it appears "the" should be --a--.

In claim 5, line 1, it appears --the-- should be inserted before "verifying" for clarity. See also claim 6, line 1. In lines 3 and 4, it appears "repeat" should be --repeating-- for consistency. See also claim 6, lines 3 and 4. In line 4, it appears --internal program-- should be inserted before "verification" for clarity and consistency (see claim 1, line 7, e.g.). See also claim 6, line 4.

In claim 9, line 1, it appears "programming" should be changed to --the programming of-- for clarity. In line 2, it appears "further" should be deleted for clarity.

In claim 10, line 1, it appears --of-- should be inserted after "programming" for clarity.

Appropriate correction is required.

6. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, and therefore its dependent claims, it is not entirely clear how a "mode" itself disables program verification. [Should --when-- be inserted after "wherein" in line 3, "disables" in line 5 changed to --is enabled,-- and --is disabled-- inserted after "memory" in line 5?]before

In claim 4, it is not clear to what "the memory internal program verification processor" refers here.

In claim 7, as well as claim 8, it is not entirely clear how simply "exiting" permanently disables an interface or enables verification (note the language of claims 20 and 21, e.g.). [Should "upon-- be inserted before "exiting" in claims 7 and 8, line 1? Should "permanently disables" in claim 7, line 2 be changed to --,-- (a comma), and --is permanently disabled-- inserted after "interface" in claim 7, line 3? Should "enables" in claim 8, line 2 be changed to --,-- (a comma), and --is enabled-- inserted after "memory (second occurrence) in claim 8, line 2?]

In claim 13, and therefore its dependent claims, the language "apparatus comprising a memory comprising ... a host processor" is somewhat confusing as the memory does not appear to "comprise" a host processor (it is not readily apparent to what "comprising" (second occurrence) refers here). [Should "comprising a memory comprising: an" be changed to --comprising: a

memory, said memory comprising an--?] Also, the relationship between the "automation circuitry" and the "special programming circuitry" is not adequately clear. [Should "disabled; a" be changed to --disabled, said automation circuitry including--, for clarity? Note Figures 4 and 5.] Also, it is not sufficiently clear to what the "circuitry to send" and "circuit to exit," which are within the "host processor," refer here, or how they are connected or related to the other elements set forth in the claim.

Applicants are respectfully reminded that while 35 U.S.C. 112 sixth paragraph permits the use of functional language in a claim, this provision must always be considered as subordinate to the second paragraph of 35 U.S.C. 112 (see *In re Lundberg*, 244 F.2d at 547-548, 113 USPQ at 534 (CCPA 1979)). If one employs functional language in a claim, one must set forth an adequate disclosure showing what is meant by that language. If applicant fails to set forth such an adequate disclosure, applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112. See *In re Donaldson Company, Inc.*, 29 USPQ 2nd 1845 (Fed. Cir. 1994).

In the instant case, the language of the specification and claims is such that applicant has failed to provide an adequate disclosure showing to what the "circuitry to send" and "circuitry to exit" refer in this instance. The terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description (in this regard, see also 37 CFR 1.75(d)(1)).

Similarly, in claim 14, it is not sufficiently clear to what the "circuitry to verify" within the "host processor" refers here. Also, the phrase "including a verification processor" is not clear in this context (what does this phrase modify?). It is also not clear how the "verification processor" is connected or related to the "host processor" of claim 13.

In claim 15, it is not clear to how the "external host processor" is connected or related to the "host processor" of claim 13.

In claim 16, the language "further including enabling" is not clear (note that this is an apparatus claim, not a method claim). The proper antecedent for "the memory internal program verification processor" is not clear.

In claim 17, the language "the verifying further includes circuitry to determine" is not clear (how does "the verifying" include "circuitry?"). Also, it is not sufficiently clear to what the "circuitry to determine" refers here, or how it is connected or related to the other elements in the claims. It is also not sufficiently clear to what the "circuitry to comparing" refers here, or how it is connected or related to the other elements in the claims. Additionally, it is not readily apparent how the "circuitry to determine" includes the second memory and "circuitry for comparing" (support for language in the specification?). The proper antecedent for "the memory" is also not entirely clear since there are two memories set forth in the claims.

In claim 18, it is not clear to what the "circuit to reprogram" refers here, or how it is connected or related to the other elements in the claims.

In claim 19, it is not clear to what the "circuit one word that did not verify" refers here.

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. 09/748,825. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned copending application claims a method and apparatus for programming a memory, the method including entering a special programming mode of a memory that disables internal program verification by the memory, the memory including automation circuitry for program verification, programming a plurality of words into the memory without the memory performing internal program verification, and exiting the special programming mode of the memory, and the deletion or removal of limitations or steps such as those directed to enabling internal program verification with the consequent loss of their function, would have been readily obvious to those of ordinary

skill in the art at the time the claimed invention was made, anticipation being the epitome of obviousness. See particularly claims 1-2, 15-16 and 22-23, for example. Note also that the commonly assigned patent also claims subsequently enabling internal program verification, as well as having a host processor verify external to the memory the programming of the plurality of data words into the memory. The commonly assigned patent also claims disabling entry into the special program mode of the memory, as well as using only a single programming pulse for each bit of each word of the plurality of words, and sending a data word to the memory for reprogramming.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 1-24 are also provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09/749,133. Although the conflicting claims are not identical, they are not patentably distinct from each other because the commonly assigned copending application claims a method and apparatus for performing programming operations in a memory as in the present invention, the method including entering a special programming mode of a memory that disables internal program verification by the memory, the memory including automation circuitry for program verification, programming a plurality of words into the memory without the memory

performing internal program verification, and exiting the special programming mode of the memory, and the deletion or removal of limitations or steps such as those directed to hashing words and comparing hash values, with the consequent loss of their function, would have been readily obvious to those of ordinary skill in the art at the time the claimed invention was made. See particularly claims 1, 14 and 17, for example. The commonly assigned patent also claims enabling internal program verification, as well as programming a plurality of words, and using a host processor as a "verification processor" to verify the programming during a special programming mode.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Intel Corporation Application Note AP-629 or AP-678, each taken separately, in view of Olivo et al.

With respect to claim 1, as well as claim 13, a method for programming a memory including enabling a "special" or test programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for program verification, was known in the art at the time the claimed invention was made. See, for example, Intel Corporation Application Note AP-629 or AP-678, each taken separately. As one of ordinary skill in the art would readily appreciate, a plurality of words may be programmed into the memory during a "special" or test mode, and the "special" or test programming mode exited after the tests are performed.

Application Note AP-629 also teaches that, in order to reduce programming and testing time of a nonvolatile memory, one should consider modifying the method or program flow to perform only necessary operations (see AP-629, at page 9, as well as page 10 and Figure 4). Application Note AP-629 further teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one can save time by not performing program verify operations (see AP-629, at page 9, column 2, e.g.).

Application Note AP-678 similarly teaches that verification of each location as it is programmed or written should be eliminated from the programming routines of automated flash memories (see AP-678, at page 9, column 1, e.g., as well as page 10 and Figure 3), since program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations (see AP-678, at page 9, column 2, e.g.).

The Application Notes only specifically discuss saving time by not performing program verify operations with the external ATE , and do not teach disabling internal program verification operations during the "special" programming mode so that a plurality of words are programmed in the "special" or test mode without the memory performing internal program verification.

Olivo similarly discloses a method of programming a memory such as a flash nonvolatile memory during a "special" or test programming mode of the memory, and teaches disabling program verification operations by an internal state machine during the "special" programming mode so that a plurality of words may be programmed or tested without the memory performing internal program verification (see column 1, lines 26-62; column 2, lines 9-31; and column 4, lines and 7-12 32-36, e.g.). Olivo teaches that overall testing speed may be improved, and that various testing values or parameters may be selected at will so that the memory test can be made fully independent of the control unit and the internal state machine (see column 5, lines 1-10, as well as column 1, lines 40-62, e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to disable program verification operations by an internal state machine during a "special" programming mode, as taught by Olivo et al, in the flash memory apparatus and method of Intel Corporation Application Note AP-629 or AP-678, each taken separately, so that a plurality of words may be programmed without the memory performing internal program verification, because the Intel Corporation Application Note AP-629 or AP-678, each taken separately, teaches that program verify operations initiated by external automatic test

equipment (ATE) are redundant with internal program verify operations and that one should consider modifying the method or program flow to perform only necessary operations, and Olivo teaches that an improved testing speed and greater flexibility in the testing process may be obtained by disabling or not performing internal program verification operations. The improvement in testing speed and ability to change the testing process independent of the control unit and internal state machine as taught by Olivo et al provide ample motivation and suggestion to disable internal program verification operations in a memory such as in the Intel Corporation Application Note AP-629 or AP-678, each taken separately, so as to avoid redundant program verify operations while providing an improved test speed and increased flexibility in the testing process.

With respect to claims 2-3 and 14-15, one of ordinary skill in the art would readily appreciate that the automated test equipment in the Intel Corporation Application Note AP-629 or AP-678, each taken separately, may include processor and that the memory may be tested by resending a plurality of words previously sent into the memory.

With respect to claims 4-6 and 8, as well as claims 16-18 and 20, internal program verification by the memory may be enabled after the memory is tested so that the user can be assured that data is being properly programmed and is reliable. The programming and testing of nonvolatile memories is an iterative process so that if one of the plurality of words does not verify, the programming and verification are repeated (see page 2, lines 15-20 of the present specification, e.g.). If all of the plurality of words verify, the programming mode may be exited.

As per claims 7 and 19, one of ordinary skill in the art would recognize that the "special" programming mode may be permanently disabled after being tested at the factory so that a user is not able to enter the "special" programming mode.

With respect to claims 9 and 21, one of ordinary skill in the art would recognize that the number of iterations in the programming or testing sequence may obviously be varied. The ability to simply change the testing procedure is a key aspect of the teachings of Olivo et al, and the selection of a single iteration or a single programming pulse in order to quickly test the memory would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made.

With respect to claims 10-12 and 22-24, the Intel Corporation Application Note AP-629 or AP-678, each taken separately, teaches that programming the plurality of words into the memory may continue until a programming ending condition is met (see page 4, line 14 to page 5, line 3 of the present specification, e.g.). As one of ordinary skill in the art would readily appreciate, the programming ending condition may be that a pre-selected time has elapsed (a "timeout" condition has occurred) or an ending address (the last address in the memory has been reached and the entire memory has been tested).

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fazio et al (U.S. '489), cited by applicants, is noted of interest as discussing saving time by not performing program verify operations (see column 2, lines 27-29 and 47-50, as well as column 9, lines 64-67).

Fazio et al (U.S. '266), is cited of interest as also discussing saving time by not performing program verify operations (see column 9, lines 58-61, e.g.) and as discussing using a single programming pulse (column 2, lines 7-9).

Jex is cited as teaching minimizing program verify time in a nonvolatile memory device similar to the present invention.

Miyawaki et al is cited as disclosing a semiconductor memory device including a "special" or testing mode similar to the present invention.

Miwa et al is cited as teaching a simplified verification process for a flash nonvolatile memory.

It is also noted here that the "Notification of Transmittal" of the International Search Report listed in the IDS filed July 16, 2002 has NOT been considered since a "Notification of Transmittal" is not a document or publication which may be considered by the Examiner for relevance to the claimed invention, and since a copy of the International Search Report itself listing the references and their relevance to the present claims was not provided. Additionally, the Application or Serial number listed at the top of one form 1449A/PTO accompanying the IDS does not correspond to this application, rendering it unclear whether the IDS was intended for the

present application or the application listed on form 1449A/PTO. [Note, however, that PCT/US01/4877 listed in the IDS appears to claim priority from this application (U.S. 09/752,594).]

Note also that the two U.S. references listed on a separate form 1449A/PTO in the IDS filed July 16, 2002 have been considered.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187